



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

REC'D
NOV 12 2004
TECH CENTER 2800

In re application of

Docket No: A7680

RAGHUNATHAN, ANAND, et al.

Appln. No.: 09/576,956

Group Art Unit: 2825

Confirmation No.: 5487

Examiner: Helen B. Rossoshek

Filed: May 24, 2000

For: A METHODOLOGY FOR THE DESIGN OF HIGH-PERFORMANCE
COMMUNICATION ARCHITECTURES FOR SYSTEM-ON-CHIPS USING
COMMUNICATION ARCHITECTURE TUNERS

SUBMISSION OF FORMAL DRAWINGS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find seventeen (17) sheets of drawings in compliance with
37 C.F.R. § 1.84. The Examiner is respectfully requested to acknowledge receipt of these
drawings.

Respectfully submitted,

Chid S. Iyer
Registration No. 43,355

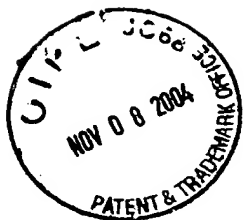
SUGHRUE MION, PLLC
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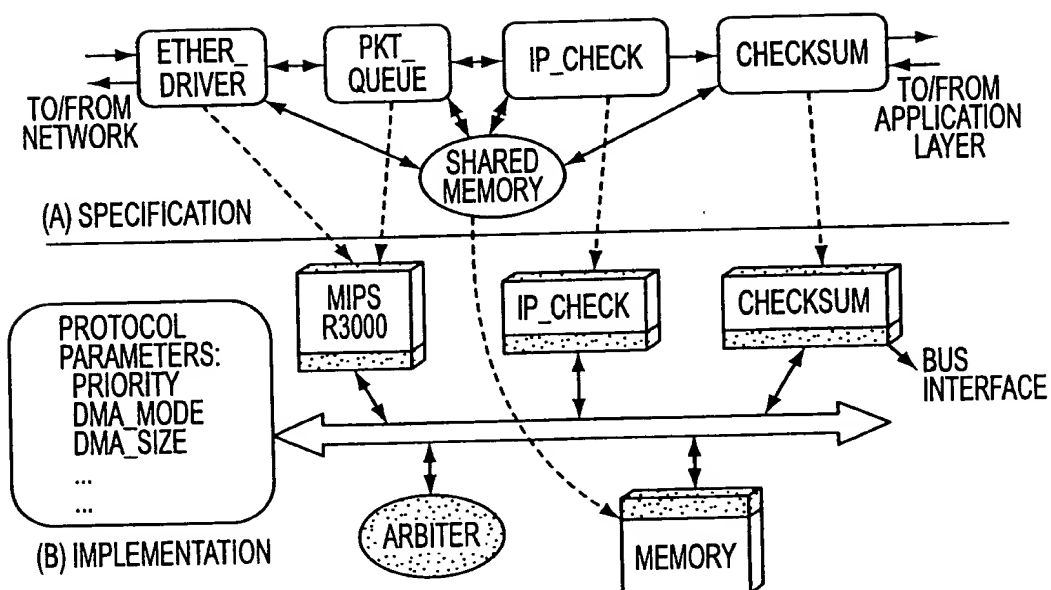
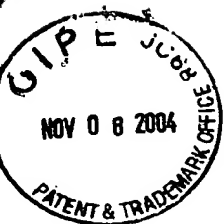


FIG. 1



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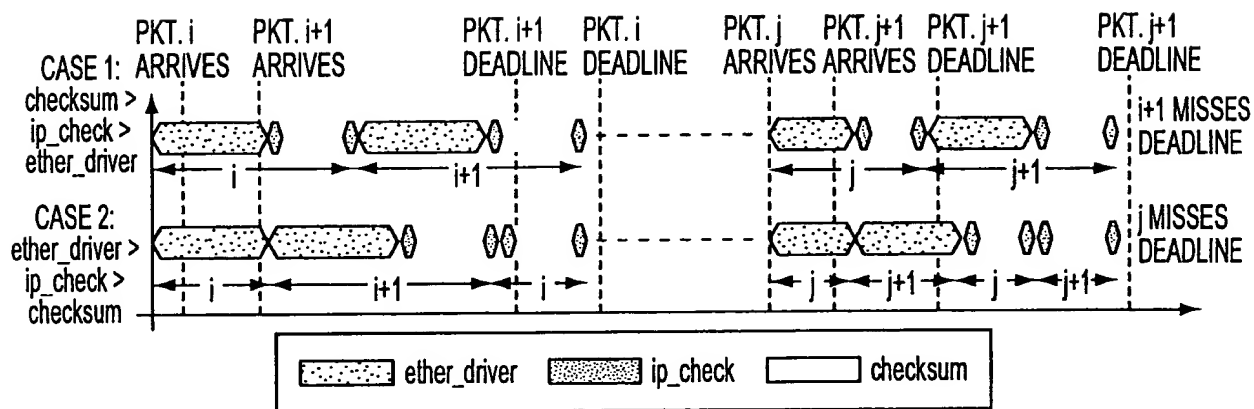
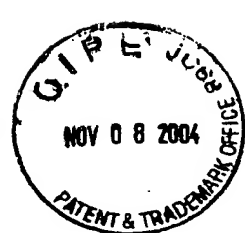


FIG. 2



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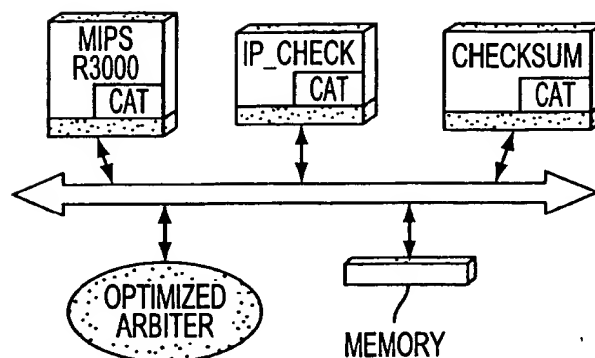


FIG. 3A

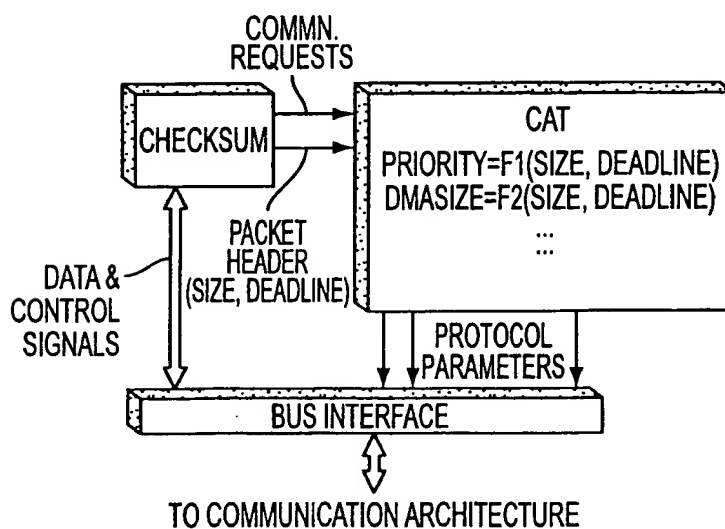


FIG. 3B



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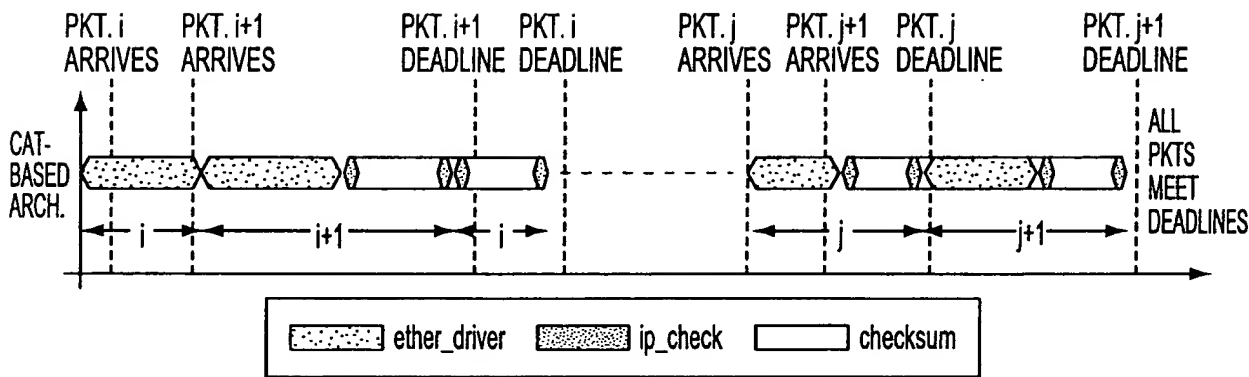


FIG. 4



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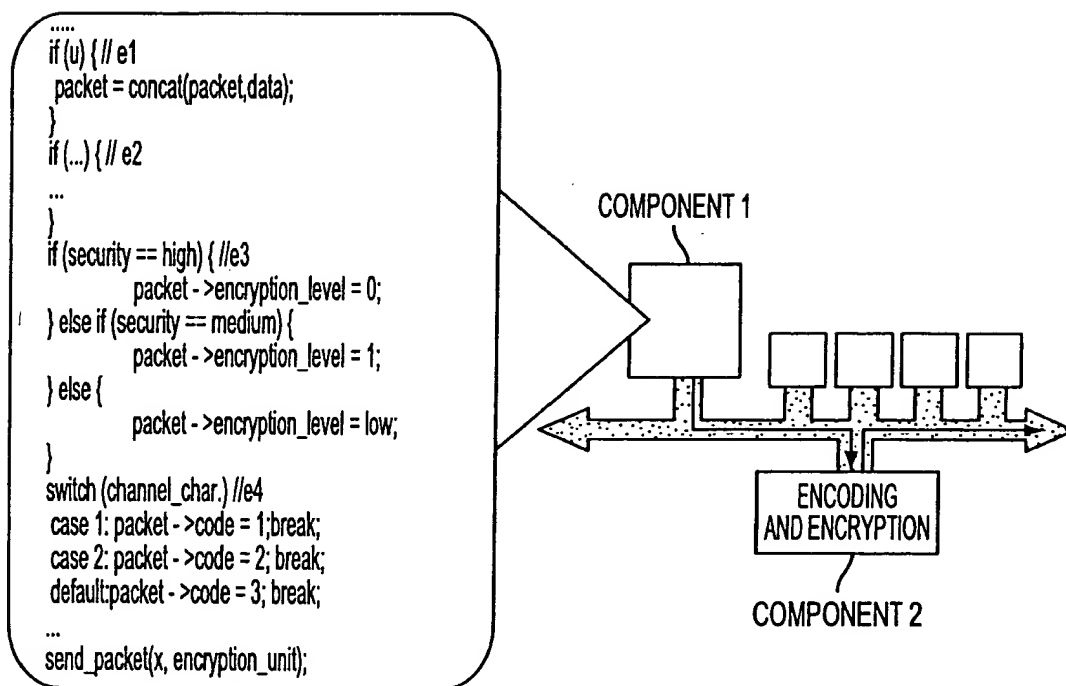


FIG. 5



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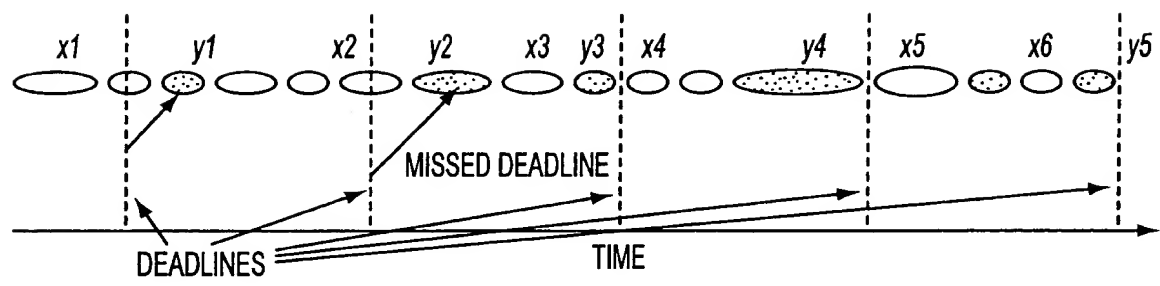


FIG. 6



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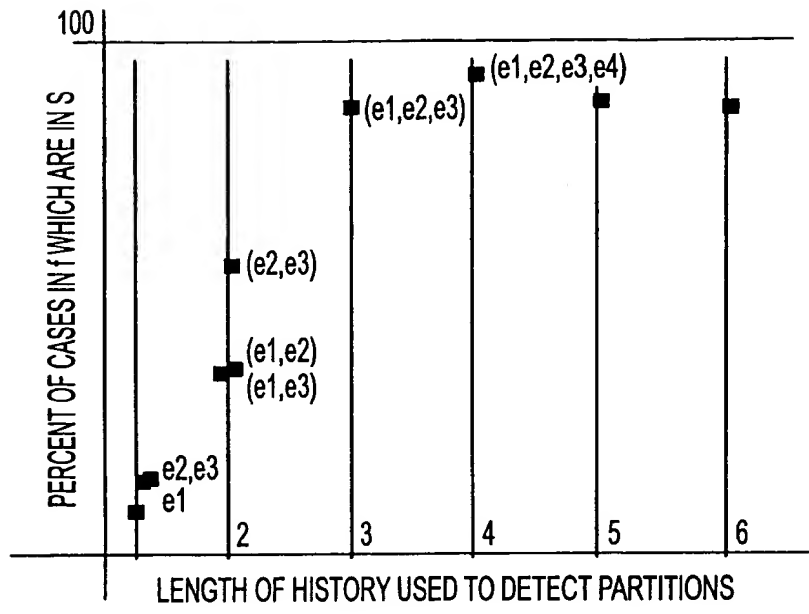


FIG. 7A

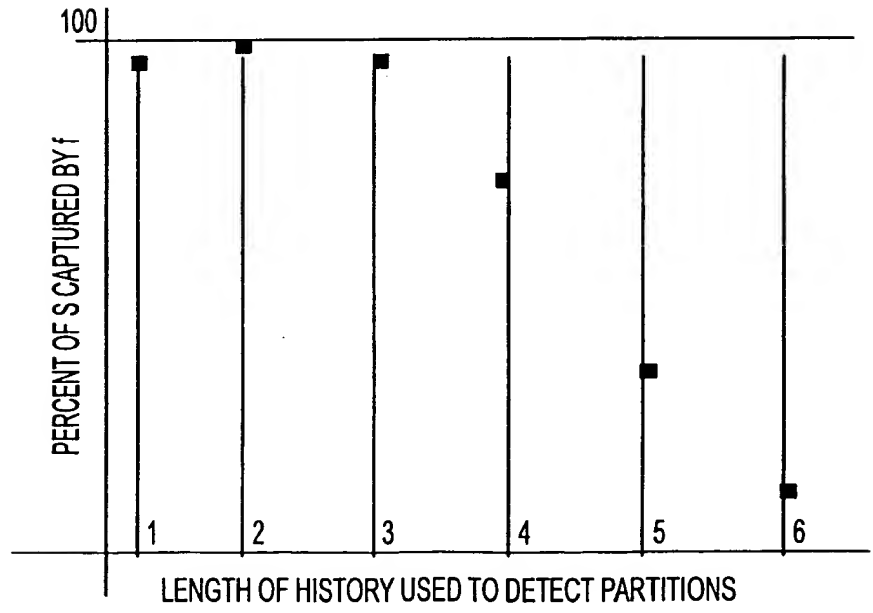
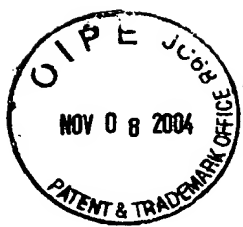


FIG. 7B



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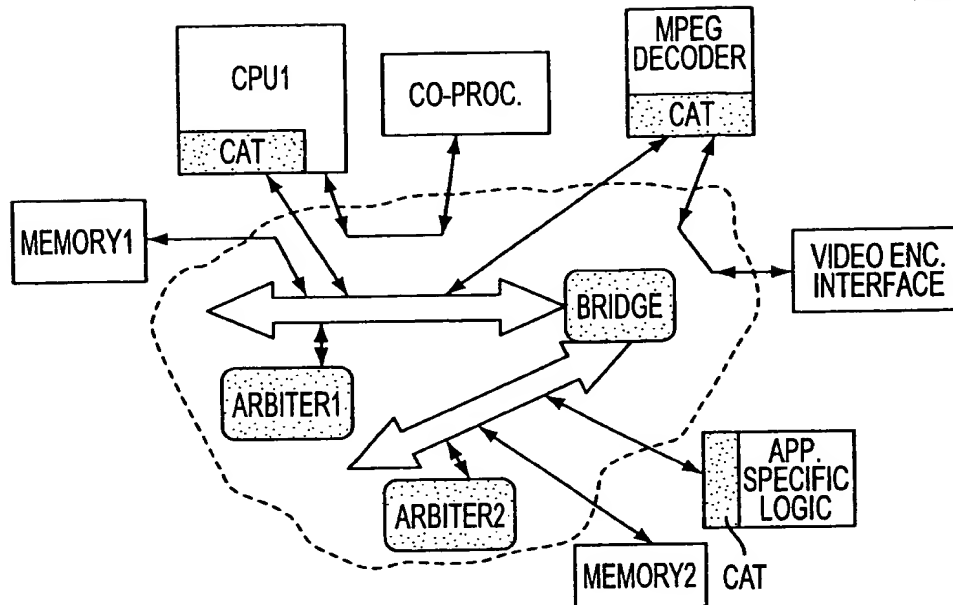


FIG. 8A

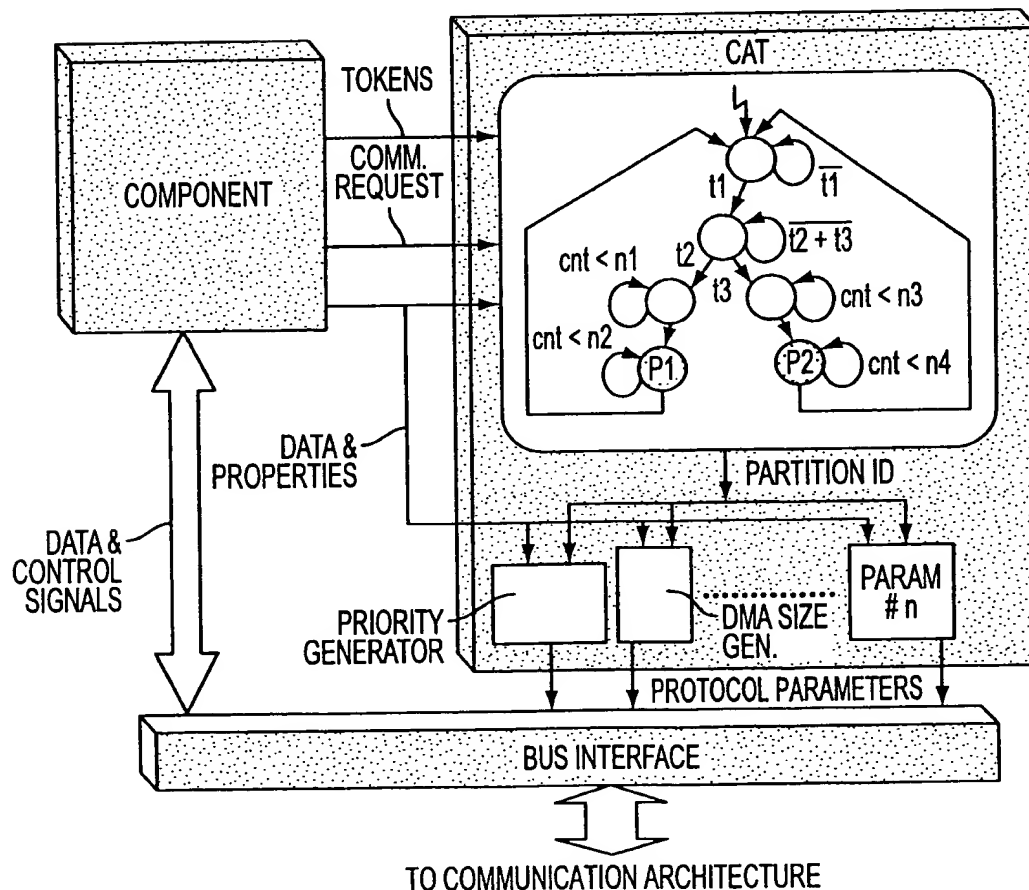


FIG. 8B



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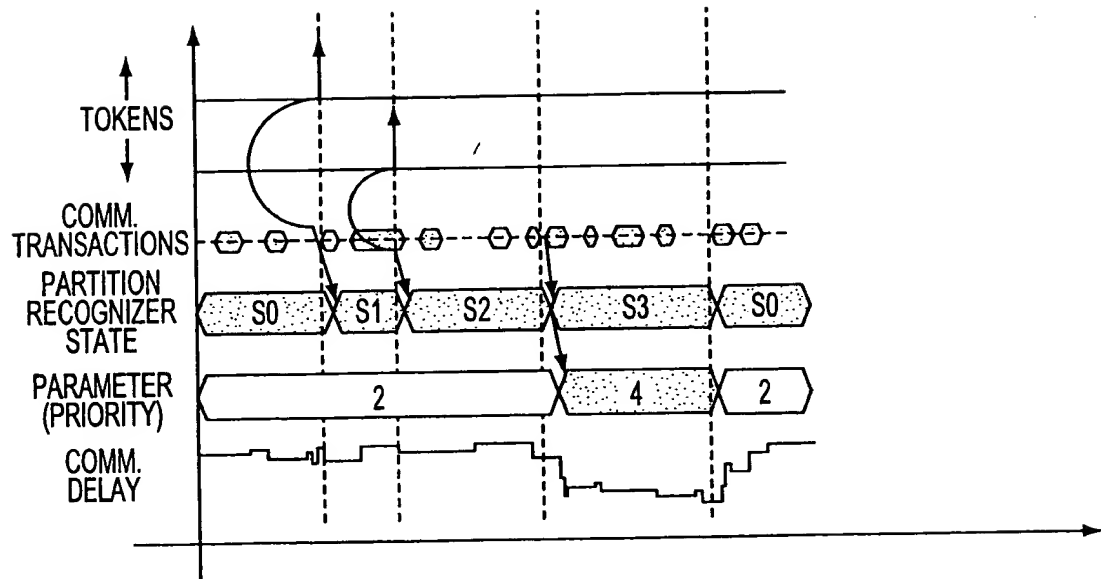


FIG. 9



EECE

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INPUTS: PARTITIONED/MAPPED SYSTEM,
COMM. ARCH. TOPOLOGY,
INPUT TRACES,
PERFORMANCE METRICS

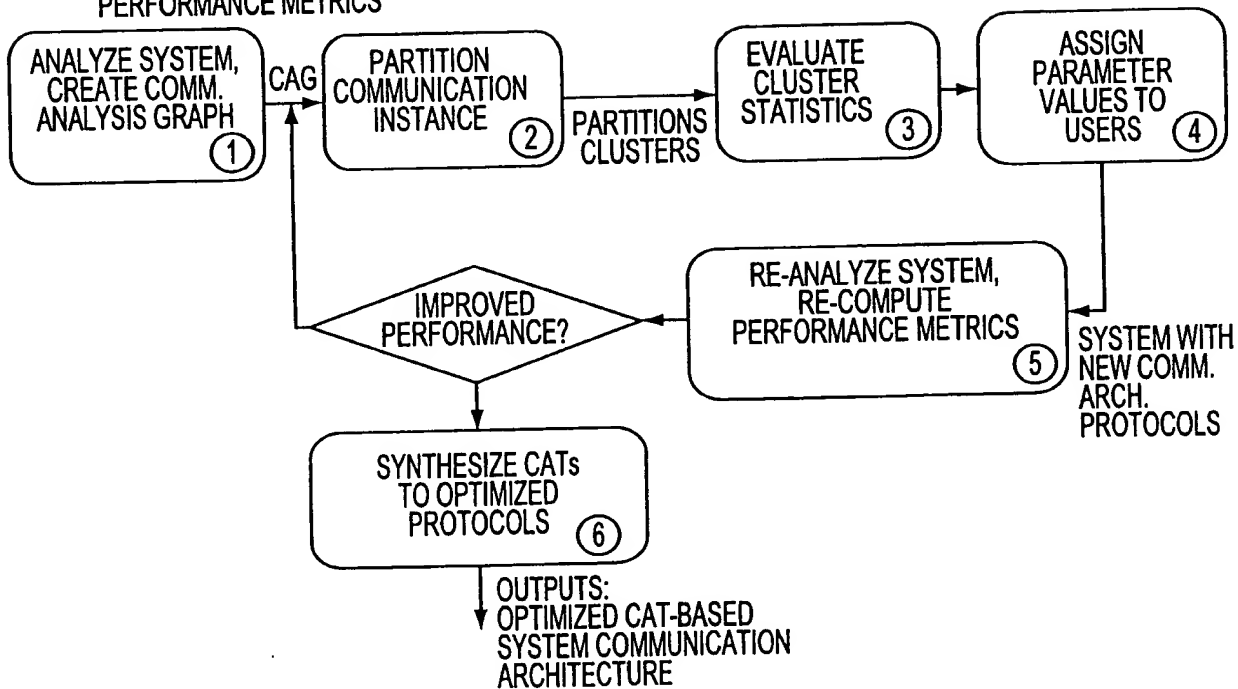
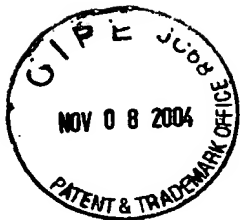


FIG. 10



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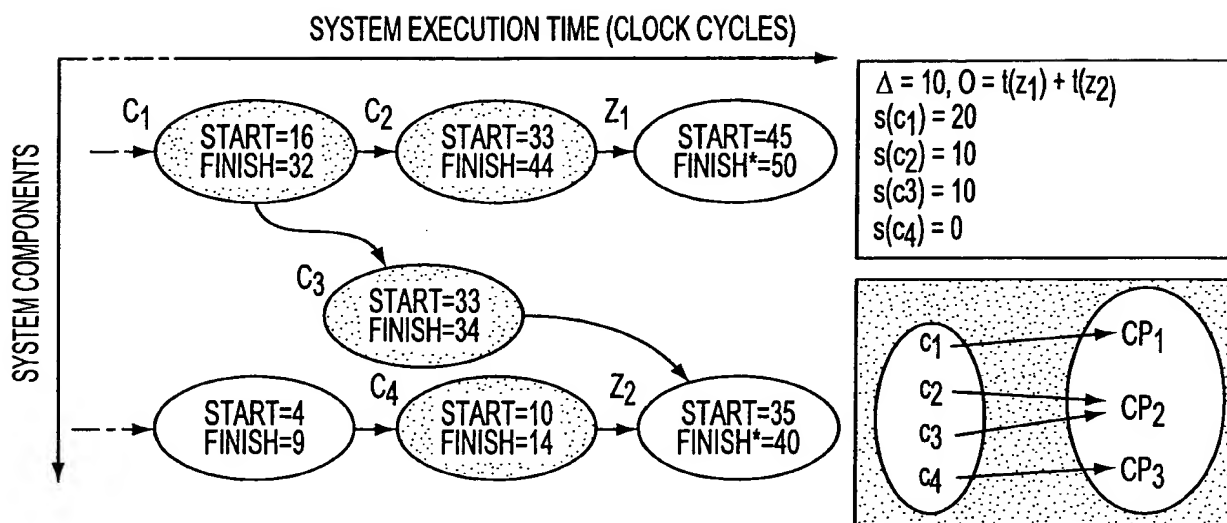


FIG. 11



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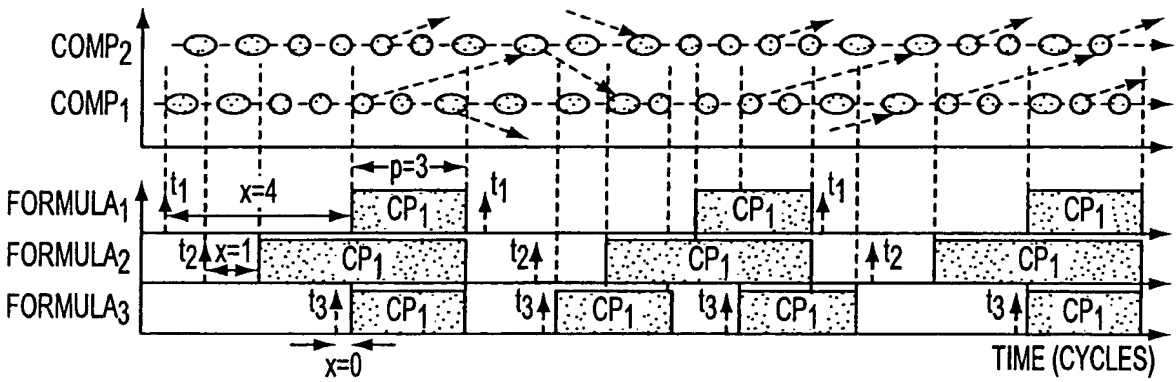


FIG. 12



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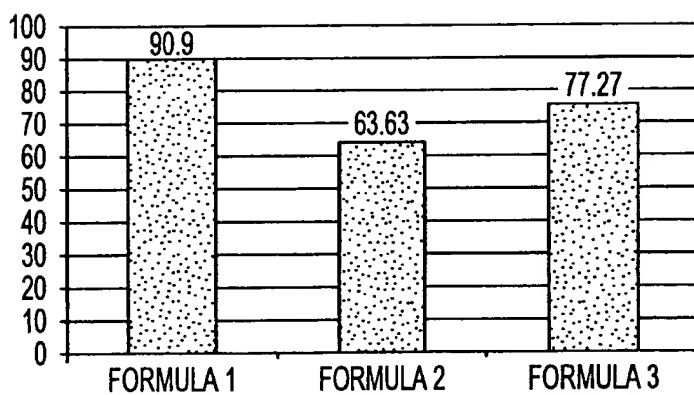


FIG. 13



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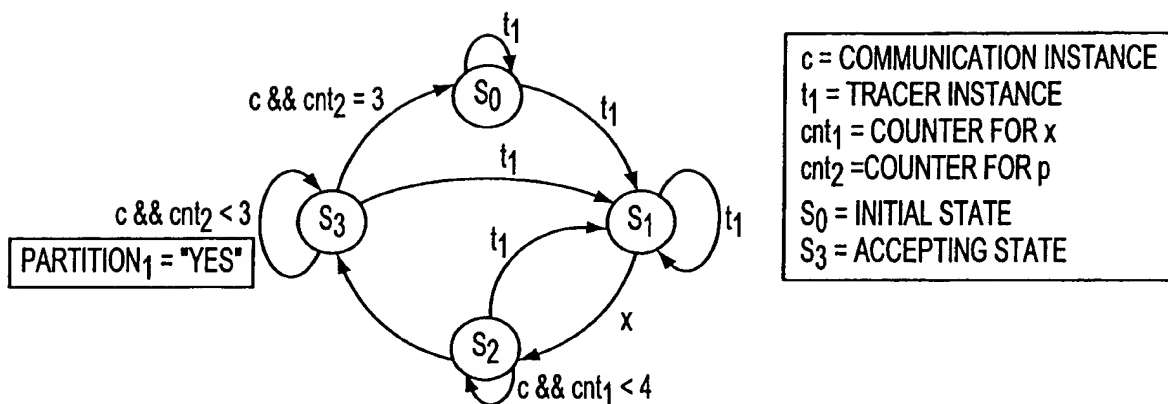


FIG. 14



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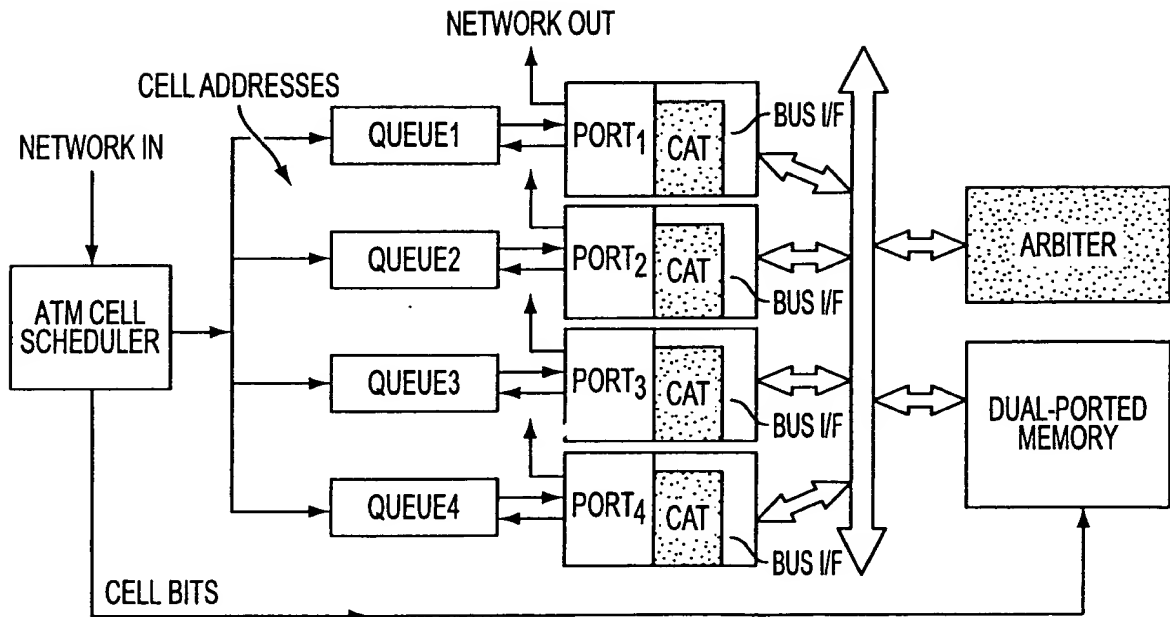


FIG. 15



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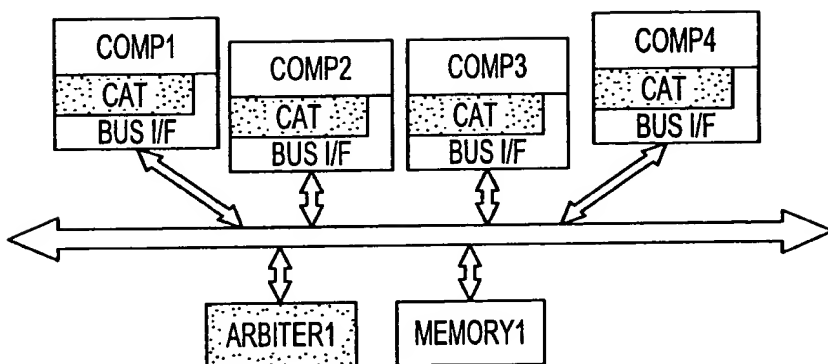


FIG. 16



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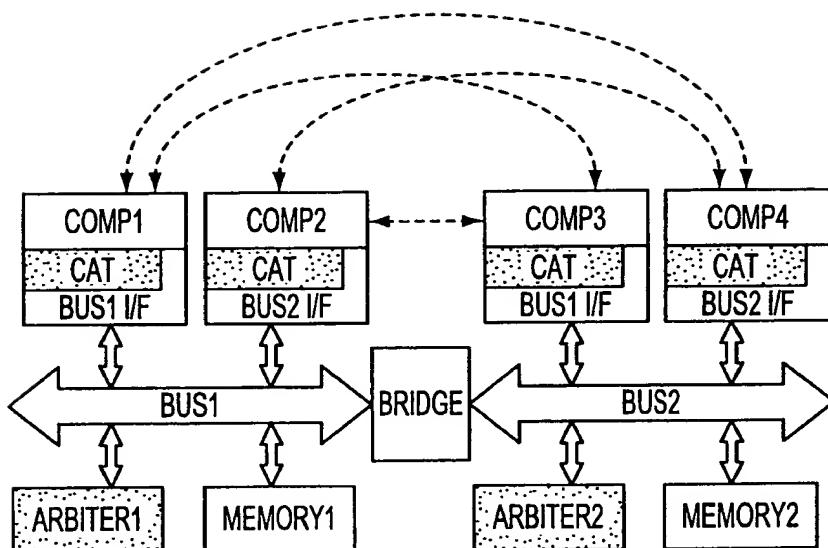


FIG. 17